

Please cancel Claims 104 - 132, 136 - 140, 145, 146, 152, 154
- 170.

Please amend Claims 133, 135, 141, 147 and 153 as set forth in amended form below:

104
1 133. (twice amended) A bidirectional data communication system
2 comprising:

3 communication signals having individual ones of a plurality of analog levels to represent information;

5 a plurality of signal lines disposed in pairs and defining a multi-pair communication environment, each signal line
6 transmitting or receiving said communication signals;

7 a transmitter block, including a plurality of transmitters, each coupled to particular ones of the signal line
8 pairs;

11 a receiver block, including a plurality of receivers, each coupled to particular ones of the signal line pairs, each receiver including;

14 an analog to digital converter configured to convert a plurality of analog levels into a corresponding plurality of digital levels defining a digital signal; and

17 a fully digital adaptive equalizer coupled to the analog to digital converter and operating on the digital signal to define information represented by the plurality of digital levels;

20 the receiver block further comprising timing recovery circuitry coupled to receive the digital signal from the analog to digital converter and extract timing information therefrom, the analog to digital converter operatively responsive to said timing information and performing digital conversions at a rate defined thereby;

26 wherein the communication signals are provided in packets, each packet comprising a preamble portion and a data

28 containing portion, the preamble portion including timing signals;

29 and

30 wherein the timing recovery circuitry comprises a first
31 timing loop having a high gain stage and a second timing loop
32 having a low gain stage, the first timing loop locking the analog
33 to digital converter in phase with the preamble portion the second
34 timing loop locking the analog to digital converter in phase with
35 the data containing portion.

104
1 135. (twice amended) A bidirectional data communication system
2 comprising:

3 communication signals having individual ones of a
4 plurality of analog levels to represent information;

5 a plurality of signal lines disposed in pairs and
6 defining a multi-pair communication environment, each signal line
7 transmitting or receiving said communication signals;

8 a transmitter block, including a plurality of
9 transmitters, each coupled to particular ones of the signal line
10 pairs;

11 a receiver block, including a plurality of receivers,
12 each coupled to particular ones of the signal line pairs, each
13 receiver including;

14 an analog to digital converter configured to convert
15 a plurality of analog levels into a corresponding plurality of
16 digital levels defining a digital signal; and

17 a fully digital adaptive equalizer coupled to the
18 analog to digital converter and operating on the digital signal to
19 define information represented by the plurality of digital levels;

20 the receiver block further comprising timing
21 recovery circuitry coupled to receive the digital signal from the
22 analog to digital converter and extract timing information
23 therefrom, the analog to digital converter operatively responsive

24 to said timing information and performing digital conversions at a
25 rate defined thereby;

26 the digital adaptive equalizer further comprising:

27 a feed forward equalizer having an input
28 receiving the digital signal from the analog to digital converter
29 and an output;

30 a slicer coupled to receive the digital signal
31 from the feed forward equalizer and outputting a signal
32 representing a symbol, the signal characterized by the digital
33 levels;

34 an adder disposed between the feed forward
35 equalizer and the slicer; and

36 a decision feedback equalizer having an input
37 receiving the signal output by the slicer and an output coupled to
38 the adder, the adder summing the output of the decision feedback
39 equalizer with the output of the feed forward equalizer.

107
1 1A1. (twice amended) A bidirectional data communication system
2 comprising:

3 communication signals having individual ones of a
4 plurality of analog levels to represent information;

5 a plurality of signal lines disposed in pairs and
6 defining a multi-pair communication environment, each signal line
7 transmitting or receiving said communication signals;

8 a transmitter block, including a plurality of
9 transmitters, each coupled to particular ones of the signal line
10 pairs;

11 a receiver block, including a plurality of receivers,
12 each coupled to particular ones of the signal line pairs, each
13 receiver including;

14 an analog to digital converter configured to convert
15 a plurality of analog levels into a corresponding plurality of
16 digital levels defining a digital signal;

17 an automatic gain control circuit coupled in
18 feedback fashion to the analog to digital converter and operatively
19 responsive to output signals therefrom to control the gain of
20 received communication signals; and

21 a fully digital adaptive equalizer coupled to the
22 analog to digital converter and operating on the digital signal to
23 define information represented by the plurality of digital levels;

24 the digital adaptive equalizer further comprising:

25 a feed forward equalizer having an input
26 receiving the digital signal from the analog to digital converter
27 and an output;

28 a slicer coupled to receive the digital signal
29 from the feed forward equalizer and outputting a signal representing
30 a symbol, the signal characterized by the digital levels;

31 an adder disposed between the feed forward
32 equalizer and the slicer; and

33 a decision feedback equalizer having an input
34 receiving the signal output by the slicer and an output coupled to
35 the adder, the adder summing the output of the decision feedback
36 equalizer with the output of the feed forward equalizer.

1 147. (amended) In a bidirectional communication system, a method of
2 processing signals received through a multi-pair transmission
3 medium, the signals having characteristic values occurring at a
4 characteristic frequency, the method comprising:

5 providing an A/D converter, coupled to receive the signals
6 from the transmission medium;

43

7 providing a sampling clock signal at a sampling clock
8 frequency equal to the characteristic occurrence frequency of
9 received signal characteristic values;

10 sampling the received signals in the A/D converter at the
11 sampling clock frequency;

12 generating signal samples at the sampling clock frequency,
13 each signal sample being output from the A/D at a time assumed to
14 correspond to the occurrence of a signal characteristic value;

15 processing each signal sample in a timing recovery circuit
16 coupled, in feedback fashion, between the output of the A/D and a
17 sampling clock input thereto;

18 determining whether the occurrence of a signal
19 characteristic value leads or lags the sampling clock signal in
20 phase; and

21 adjusting the phase of the sampling clock signal such that
22 each signal sample is output from the A/D at a time that actually
23 corresponds to the occurrence of a signal characteristic value, a
24 sampling clock phase thereby being locked to a corresponding phase
25 of a signal characteristic value;

26 wherein the received signals are analog signals disposed
27 in packets, each packet of the analog signals disposed in packets
28 being divided into a first packet region comprising timing signals
29 and a second packet region comprising data signals, the method
30 further comprising:

31 sampling the received data signals in the A/D converter
32 at the sampling clock frequency, wherein the data signals are
33 sampled after the phase of the sampling clock signal has been locked
34 to the phase of a signal characteristic value of the timing signals.

1 153. (amended) In a bidirectional communication system, a method of
2 processing analog signal packets received through a multi-pair
3 transmission medium, each analog signal packet including a plurality

4 of signals having characteristic values occurring at a
5 characteristic frequency, the method comprising:

6 providing a sampling clock signal at a sampling clock
7 frequency equal to the characteristic occurrence frequency of
8 received signal characteristic values;

9 predicting an occurrence time corresponding to the
10 characteristic occurrence frequency of received signal
11 characteristic values;

12 sampling the received signals at the sampling clock
13 frequency and at the predicted occurrence time to thereby generate
14 signal samples at the sampling clock frequency, each signal sample
15 assumed to correspond to the occurrence of a signal characteristic
16 value;

17 processing the signal samples in a high gain error
18 generator, the high gain error generator determining whether the
19 occurrence of a signal characteristic value leads or lags the
20 sampling clock signal in phase; and

21 adjusting the phase of the sampling clock signal such that
22 each signal sample is generated at a time that actually corresponds
23 to the occurrence of a signal characteristic value, the sampling
24 clock having an occurrence time locked in phase with a corresponding
25 occurrence of a signal characteristic value;

26 the signals of each analog signal packet being
27 characterized by a plurality of analog amplitude values, the values
28 of the analog amplitudes defining information content, the method
29 further comprising:

30 dividing each analog signal packet into a first packet
31 region comprising timing signals and a second packet region
32 comprising data signals; and

33 converting the analog amplitude values of the data signals
34 to digital representations thereof by an A/D converter after the
35 occurrence time of the sampling clock signal has been locked to the